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An ANN Based Capicitor Voltage Balancing Method For Neutral Point Clamped Multi-Level Inverter

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Abstract
Multi-level inverters are became popular for usage in medium voltage, low voltage power applications due to flexibility in control and better performance characteristics in terms of harmonic regulation. Neutral point clamped are popular as they require less number of sources as their input when compared with their counter parts i.e. cascaded multi-level inverters and found to be reliable when compared with flying capacitor based multi-level inverters. But when neutral clamped technologies are used for generation of three-phase voltages, the capacitors that are connected at input side experiences imbalance in their voltages, this makes neutral point clamped multi-level inverters less reliable. In the proposed work an attempt is made to study circuits that balances the capacitor voltages and a scheme is investigated for balancing the capacitor voltages. Method proposed in [1] uses PID controller for balancing the capacitor voltages. In this project PI based control scheme and artificial neural network (ANN) based control scheme for the front end circuit shown in [1] are designed for achieving balance among the capacitor voltages. The proposed control scheme is simulated with the help of Simpowersystems block set and neural network toolbox of MATLAB software for different load conditions. Results obtained from ANN based controller and PI controller are presented.

Keywords—DC Volatge balance, Neutral Point Calmaped Multilevel Converter, Multilevel Converetrs, ANN based Controller.

I. INTRODUCTION

Multilevel converters (MLC) have the later years been looked upon as a decent choice for medium- and high-voltage applications. It had been first given in [2]. Before the introduction of multilevel converters the standard answer has been to attach semiconductors asynchronous switches to resist the high voltages. This needs fast change to avoid unequal voltage sharing between the devices that may lead to a breakdown. MLC have the advantage of clamping the voltages that prevents the necessity of quick change. MLC even have a smoother output voltage than traditional two-level converters.

Multilevel inverters have an arrangement of switches, capacitors and voltage sources for production of stepped sine wave output at their output terminals. By using proper control, the switching devices can generate stepped output voltages with low harmonic distortions. Multilevel inverters have drawn tremendous interest in the field of medium, high-voltage and high-power applications because it has some advantages: it can realize high voltage and high power output using low-voltage switches without use of transformer and dynamic voltage balance circuits. With increased output levels reduced harmonics are produced. Most commonly used multilevel inverter configurations are diode-clamped, capacitor-clamped and cascaded H-bridge inverters.

Among the available basic multilevel inverter configurations, the problem of voltage unbalance of dc link capacitors exist in diode-clamped inverter topology. Due this reason usage of diode-clamped inverters for production of high voltage levels is limited.

Diode-clamped converter topology is also known as neutral-point-clamped converter (NPC).This topology was proposed in the early 80's by [9], multilevel power converters are being employed in the industry, mainly in high-power applications [10]. Bi-directional power flow, near sinusoidal currents and high efficiency are some of the most attractive features that these power conversion systems have. Each phase of a multilevel converter can generate more than two different voltage levels. When compared with the conventional two-level converter, the generated voltages have more possibility to approach the sinusoidal waveforms, which reduces the harmonic distortion [11]. But increase of number of voltage levels leads to a higher complexity in converter structure and require additional dc-link

capacitors in topologies such as the NPC. Concerning these capacitors, balancing of their voltages according to operating point is one of the major technical challenges of multilevel converters.

In a NPC based three-level inverter, the DC-link voltage is shared by the capacitors, Unbalance of neutral voltage is caused due to the current flowing into and out of neutral point. Unbalance of potential of neutral point is an inherent problem in NPC inverters. Neutral point voltage unbalance can be attributed to non-uniform voltage distribution of DC-link capacitor voltages, operating conditions and load types. Unbalance in neutral point voltage increases harmonics in output voltage, may drift the output voltage to an unacceptable level, which in turn lead to damage of the switching devices and filter capacitors [17]-[21]. In literature various control strategies have been proposed to maintain the balance of neutral point voltage. A zero sequence signal is added to modulation waves in Sinusoidal Pulse Width Modulation Scheme (SPWM) in order to balance the neutral point voltage [22]. This requires separate measuring circuit for measurement of power factors and phase angle of load voltages and currents. To balance the voltage of dc link series capacitors, several approaches have been proposed. Some of them are: 1) Using separate dc sources, [3], [4] 2) Adding some auxiliary balancing circuits [5], [6] and 3) Improving the control method by selecting redundant switching states [7], [8].

By using auxiliary circuits, the transferred current or power accurately controlled, these circuits require additional feedback control strategies, so the control of these converters becomes more complicated, and this feature makes these inverters less reliable for usage in medium, high –voltage applications.

A scheme is proposed in [23] uses less number of measuring quantities for design of control circuit but the drawback is instantaneous control is not possible. Scheme proposed in [24] is valid only for those circuits in which the change in neutral voltage is proportional to change in carrier signals. So, a three-level boost converter (TLBC) is presented and used as an active front end circuit for a three-phase five level neutral point clamped multilevel inverter. The switches shown in circuit are controlled with PI based PWM control scheme. The TLBC circuit is consisting of three-level boost converter and four capacitors. The capacitor voltage balancing in the five-level NPC MLI is done by TLBC i.e., all the capacitor voltages are equal to the 1/4th of source voltage. But for betterment working and better quick response and settling time of capacitor voltages artificial neural network (ANN) based switching scheme is used in place of PI controller.

The working of NPC based MLI is discussed in section II followed by working of TLBC. The TLBC actually consists of PI controller for capacitor voltage balancing which in turn replaced by an ANN. The working of TLBC and ANN are also discussed in section II. Section III presents modeling aspects of ANN based switching scheme.

II. PRINCPLE & OPERATION

A. Neutral point Clamped Multi level Inmverter – Principle & Operation

A NPC based multilevel inverter mostly consists of(m-1) capacitors on the dc bus and produces m levels on the phase voltage. The following Fig.2.1 shows you the three-phase five-level NPC. The order of the switches is S_1, S_2, S_3, S_4, S_5, S_6, S_7 and S_8 and as it is a five-level converter it consists of 4 capacitors namely C_1, C_2, C_3 and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$. So an m-level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1) (m-2) clamping diodes.

The figure shown in 2.1 is one leg of the three-phase five-level NPC. The arrangement of steps to blend the five-level voltages is as follows:

- For an output voltage level $V_{ao} = V_{dc}/2$ turn on all upper half switches S_1 through S_4.
- For an output voltage level $V_{ao} = V_{dc}/4$, turn on three upper switches S_2 through S_4 and one lower switch S_5.
- For an output voltage level $V_{ao} = 0$, turn on upper two switches S_3 and S_4 and two lower switches S_5 and S_6.
- For an output voltage level $V_{ao} = -V_{dc}/4$, turn on one upper switch S_4 and three lower switches S_5 through S_7.
- For an output voltage level $V_{ao} = -V_{dc}/2$, turn on all lower switch S_5 through S_8.

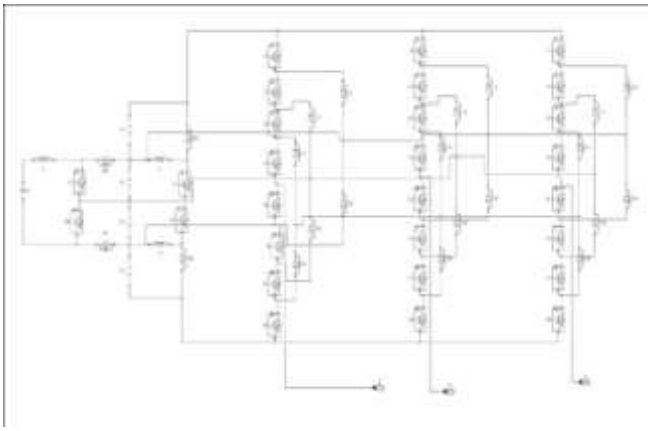

Fig.2.1: Schematic circuit of Three-level boost chopper based 5-Level NPC inverter.

The following table 2.1 shows the NPC based MLI output voltage level for their relevant switching samples. State condition 1 means the switch is on, and state condition 0 means the switch is off. It should be noticed that each switch is turned on only once per cycle and there are four complementary switching pairs in each cycle. The pairs mentioned here are for one leg of the three-phase five-level NPC. They are (S1, S5), (S2, S6), (S3, S7) and (S4, S8).thus, if one of the complementary switches is on, then the other switch of the same pair must be off. Four switches are at on state always at the same time.

Table.2.1: Switching state of the five-level NPC:

Pole Voltage (V_{AO})	Switching states							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

This circuit configuration provides excellent control over power flow and most preferred study in real time applications [25-30] which addresses the important issue of unequal allocation of voltages in clamping diodes in neural point clamped converters with higher number of levels.

B. Three-level Boost Converter(TLBC)-Working and Operation

It has long been familiar that, for the NPC inverter with more than three levels, a static front-end capacitor voltage balancing method is only achievable if the modulation index is limited to about 60% of its maximum value for loads with a typical 0.8 power factor [38]–[41].

If the modulation index is raised greater than this worth, the inner capacitors gradually discharge, and sooner or later, the inverter output converges at three stages [42]. To beat this drawback, a multilevel inverter can also be offered with the remote dc sources [37], [43] similar to the outside circuit as the active front-end solution of dc-link capacitor balancing [38], [42], [44]–[47], making use of balancing circuit by transferring charge from one capacitor to another capacitor to equilibrium stage [33], [34], [48] or the change of the pulse width modulation (PWM) switching sample [31], [32], [35],[36], [39],[49]–[53].

Many authors proposed PWM techniques for capacitor voltage balancing to avoid additional cost when using active front end balancing circuit. This process is observed to have problem on the range of operation with the changing of the power factor and modulation index [40], [41] and [50]. Once a PWM technique is employed for dc-link capacitor voltage balancing, solving problems such as total harmonic distortion, common-mode voltage cancellation, and leakage current elimination with the same procedure shouldn't be feasible. It has been pointed out within the introduction of [54] that capacitor voltage balancing and common mode voltage cancellation cannot be fulfilled concurrently in a multilevel inverter. On this paper, a three-level boost converter (TLBC) is used to supply a five-level neural-point-clamped inverter as proven in Fig.2.2.

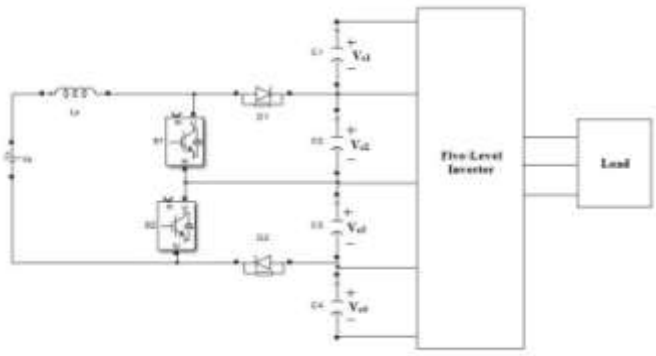

Fig.2.2: Schematic ofThree-Level boost chopper for 5-Level NPC inverter.

In energy conversion approach, a boost chopper is recurrently used as a result of its easy topology and control method [44]–[46], [55]. The TLBC has advantages in high power applications comparable to reduced switching losses and low reverse recovery losses of the diode [44]. With decreased inductor current ripple in TLBC, a smaller size inductor can be utilized in TLBC compared to the typical boost converter [47].

DC-link capacitor voltage balancing is carried out utilizing a blend of active front-end and balancing circuits. TLBC is used to balance the two inner capacitors, C1 and C2, and another balancing circuit is used to balance the outer capacitors, C1 and C4. The capacitor voltage balancing is done by transferring the charge from inner capacitors to the outer capacitors. The proposed configuration is compatible for a grid-related PV approach which operates in unidirectional power flow. The prototype is verified for various load power aspect conditions to assess its performance at a high modulation index.

C. Balancing of capacitor voltages of TLBC using ANN

1) Introduction to ANN

Work on synthetic neural network has been motivated from its inception by the consciousness that the human brain computes in a wholly specific method from the typical digital computer [56]. The brain is an extremely difficult, nonlinear and parallel information processing system. It has the potential to prepare its structural elements, often called neurons, to be able to participate in specific computations regularly rapid than the quickest digital computer in existence in these days. The brain sometimes accomplishes perceptual recognition tasks, e.g. recognizing a well-recognized face embedded in an unfamiliar scene, in approximately 100-200ms, whereas tasks of a lot lesser complexity may take days on a regular computer. A neural community is a laptop that is designed to lay out the way in which where the brain performs a special assignment. The network is implemented through utilizing electronic components or is simulated in software on a digital computer. A neural community is a vastly parallel distributed processor made up of simple processing units, which has a common propensity for storing experimental abilities and making it to be had to be used. It resembles the mind in two respects: 1) Knowledge is attained by using the network from its atmosphere by a training process. 2) Interneuron connection strengths, often called synaptic weights, are used to store the attained knowledge.

Neural networks, with their amazing potential to derive that means from problematic or imprecise information, can be used to extract patterns and observe trends that are too difficult to be observe by either people or different computer strategies. Other benefit consists: 1) Adaptive learning: An ability to learn tips on how to do duties depend on the data given for training or preliminary experience. 2) Self-organization: An ANN can create its own organization or representation of the information it receives throughout learning time. 3) Real Time Operation: ANN computations can also be implemented in parallel, and certain hardware gadgets are being designed and manufactured which take benefit of this capability.

The human nervous system can be dividedinto three stages that canbe definedas follows:

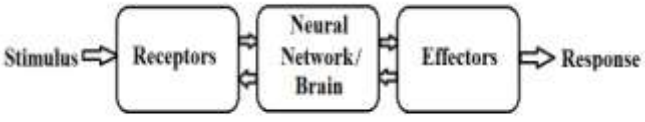

Fig 2.3: Block diagram representation of human nervous system

The receptors acquire information from the atmosphere. The effectors generate interactions with the environment e.g. activate muscles. The drift of knowledge/activation is represented by using arrows in fig.2.3.

There are roughly 10 billion neurons in the human cortex. Each biological neuron is hooked up to several thousands of other neurons. The common operating pace of biological neurons is measured in milliseconds. Nearly all of neurons encode their activations or outputs as a series of brief electrical pulses. The neuron's nucleus includes the incoming activations and converts them into output activations. The neurons nucleus includes the genetic material within the form of DNA. This exists in most types of cells. Dendrites are fibers which emanate from the cell body and furnish the receptive zones that acquire activation from other neurons. Axons are fibers appearing as transmission lines that ship activation to different neurons. The junctions that enable signal transmission between axons and dendrites are referred to as synapses

2) Training of Artificial Neural Networks

A neural network must be configured such that the application of a set of inputs produces (either 'direct' or through a relaxation system) the required set of outputs. Various ways are there to set the strengths of the connections exist. A technique is to set the weights explicitly, utilizing a priori potential. Yet another method is to train the neural network through feeding it instructing patterns and letting it exchange its weights according to a few training rule.

III. IMPLEMENTATION OF ANN BASED CONTROL SCHEME

In out proposed circuit, the error generated while comparing instantaneous capacitor voltages with reference magnitude in TLBC is given as input to an artificial neural network based controller shown in Fig-3.1. The controller is trained with a set of inputs and target outputs. The trained network is validated with different sets of known inputs. The output of ANN controller gives required modulating signal for generation of hysteresis based PWM signals for usage in active front end circuit.

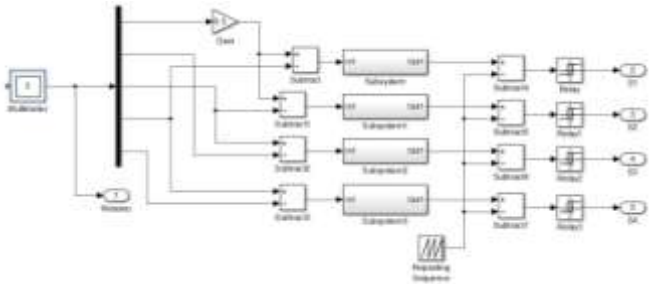

Fig.3.1: Schematic diagram of ANN based capacitor voltage control circuit

When the proposed ANN is replaced with PI controller,same like the above the error and change in error is given as the input. The error is nothing but the voltage difference between reference voltage and Vc3 for gate signal S1, voltage difference between reference voltage and Vc2 for gate signal S2, voltage differences between Vc2 and Vc1 for gate signal S3 and voltage differences between Vc3 and Vc4 for gate signal S4. The change in change in error is nothing but the dv/dt of the error as shown in the Fig.3.2. For four switches there will four ANN blocks, but all the ANN blocks will be in same structure. So, one of the ANN block is shown below in Fig.3.2.

The ANN block shown in Fig.3.2 is simulated from the NFTOOL from the MATLAB. In the NFTOOL box training of the network is initiated, the training, validation and testing percentages so that the ANN iterations depending on the percentage values. Here ANNis trained in NFTOOL by keeping 80% training, 10% validation and 10% testing with 10 hidden layers. After the NFTOOL simulates the required ANN block, then it kept in place of PI controller. The output of the ANN block generates the required modulating signals to trigger the switches. For 4 switches there will four ANN blocks simulated by NFTOOL. When the output of the ANN is compared with PI controller, it is clearly observed that ANN has the better output, better response, quick settling time f capacitor voltages. The results of both PI controller and ANN controller out puts are shown in next chapter.

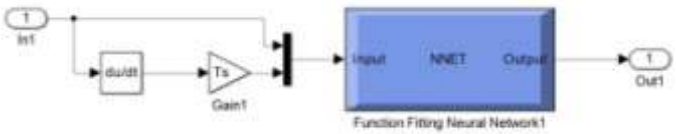

Fig.3.2: Schematic diagram of ANN block in subsystem

Each ANN block contains the following circuit in it as shown in fig.3.3. It contains variable type of limits.

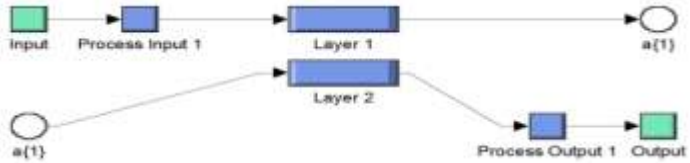

Fig.3.3: Schematic of the ANN block scehemetic diagram

For each ANN block input i.e., error and change in error from capacitor voltages is given as input to the ANN block. These error and change in error values are in range of 10,000 values and are given to NTOOL training.

IV. RESULTS

For balancing the capacitor voltages of the TLBC is done by using PI controller. To get the better performance PI controller scheme is replacing with ANN scheme. By introducing the ANN controller, it clearly observed that the response of the NPC multilevel inverter is much better and has quick settling time. The capacitor voltages reach to steady state in less time when compared to the capacitor voltages when PI controller based switching scheme is used for NPC multilevel inverter.

Case studies are performed on ANN based NPC multilevel inverter for different power factors of load and the observations are tabulated in table 4.1.Table 4.1 shows the power factor values for various load inductances and THD in the output voltages and currents. For all cases, capacitor voltages of the TLBC, output voltages and currents are recorded.

Results shown in fig.4.1 and 4.2 are the voltage across the load and current through the load connected to the NPC multilevel using PI controller.Results shown in fig.4.3 is the TLBC switching triggering circuit and the results shown from fig.4.4 to fig.4.7 are capacitor voltages.

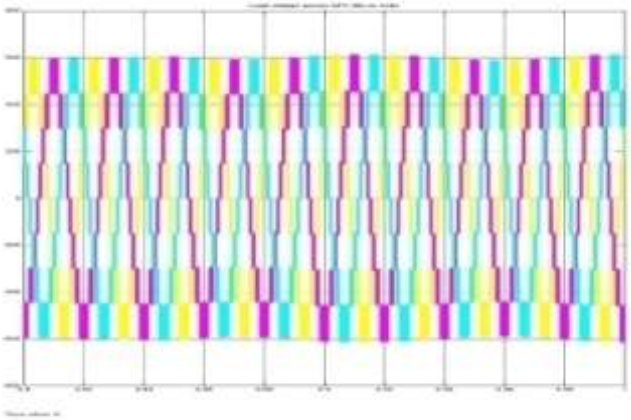

Fig.4.1: Voltage across the NPC multilevel inverter using PI controller

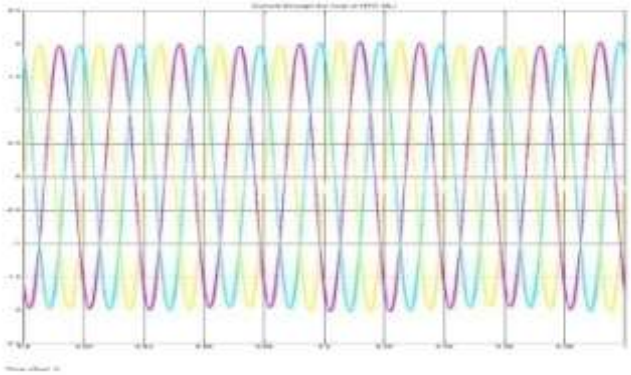

Fig.4.2: Current through the load of NPC using PI controller

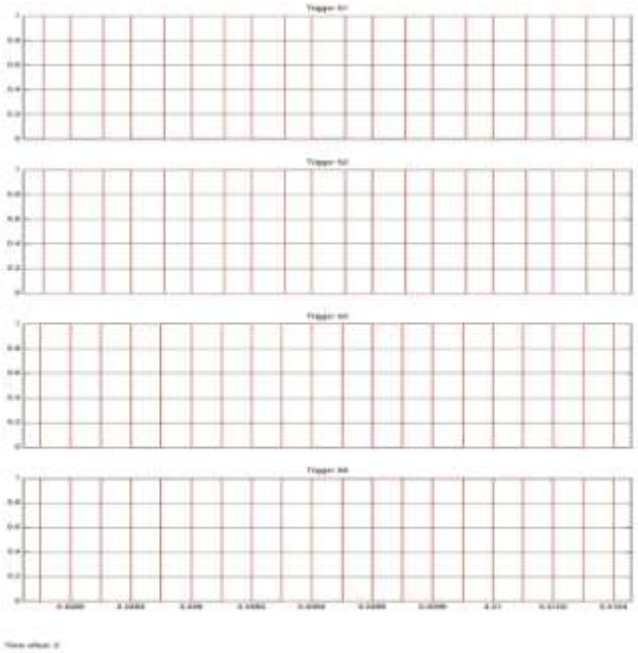

Fig.4.3: TLBC switches triggering schematic diagram when PI controller is used.

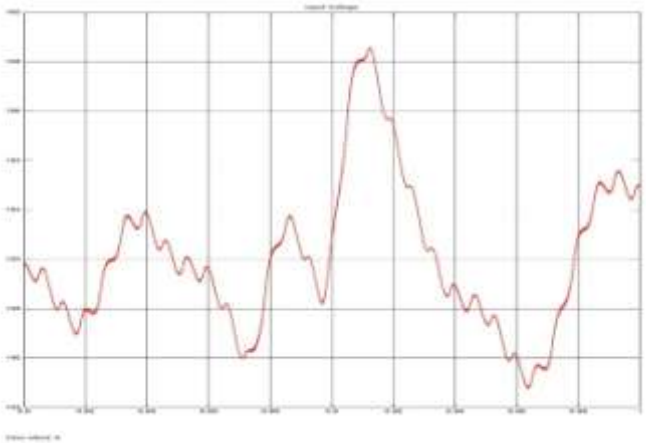

Fig.4.4: Output wave forms of capacitor voltages C1 balanced by PI controller.

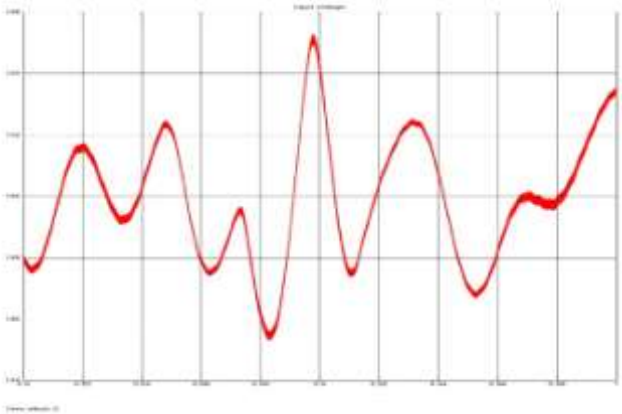

Fig.4.5: Output wave forms of capacitor voltages C2 balanced by PI controller.

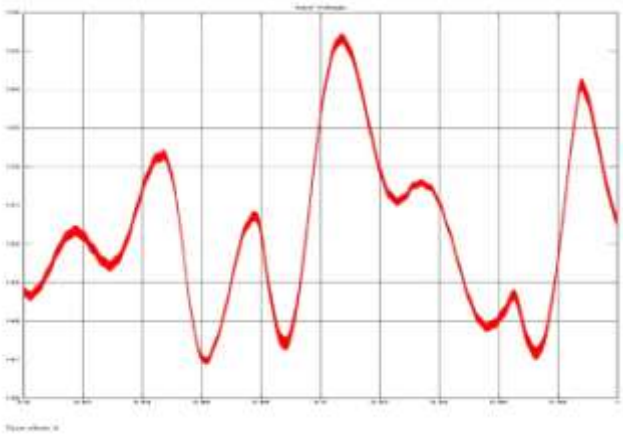

Fig.4.6: Output wave forms of capacitor voltages C3 balanced by PI controller.

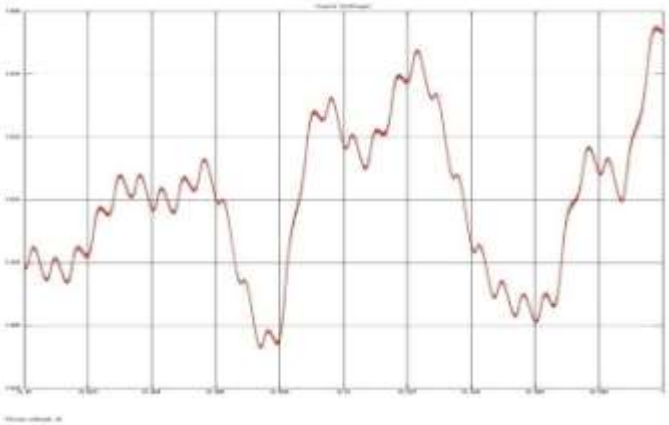

Fig.4.7: Output wave forms of capacitor voltages C4 balanced by PI controller.

Results shown in fig.4.8 and 4.9 are the voltage across the load and current through the load connected to the NPC multilevel using ANN controller. Results shown in fig.4.10 is the TLBC switching triggering circuit and the results shown from fig.4.11 to fig.4.14 are capacitor voltages.

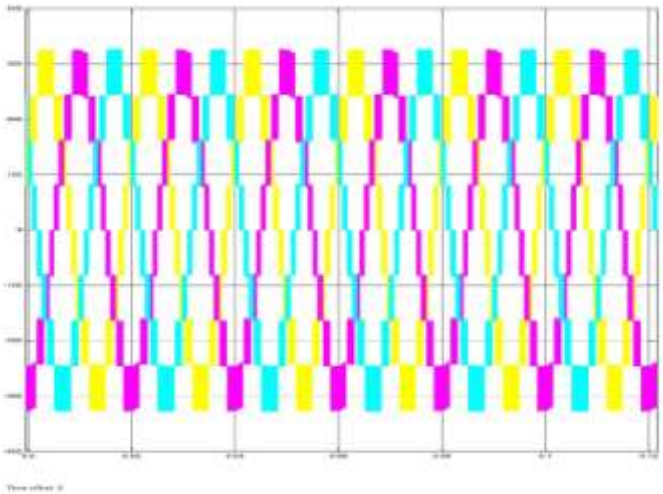

Fig.4.8: Voltage across the NPC multilevel inverter using ANN controller

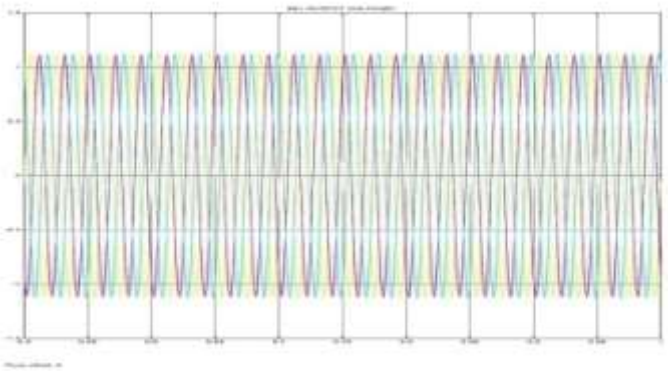

Fig.4.9: Current through the NPC multilevel inverter using ANN controller.

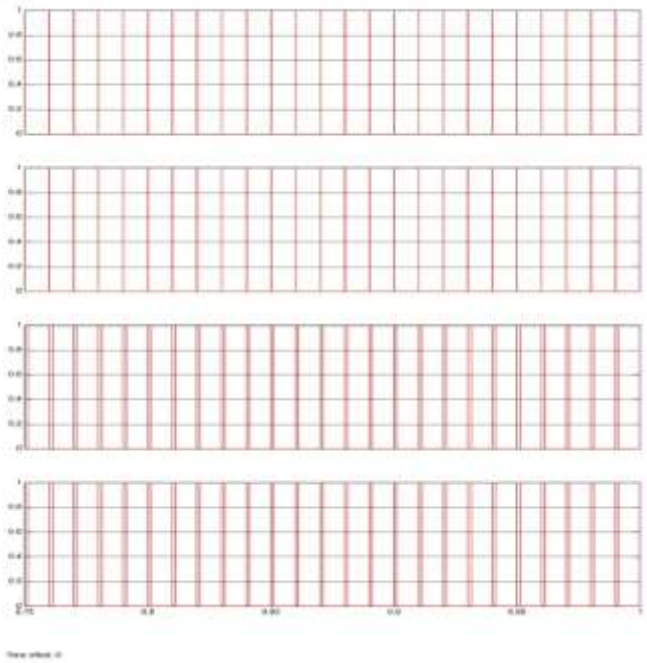

Fig.4.10: TLBC switches triggering schematic diagram when ANN controller is used.

Table.4.1: Case studies of the ANN controlled NPC multilevel inverter.

Sl.No	Power factor of Load (PF)	THD of the NPC voltage across the load (%)			THD of the NPC current through the load (%)		
		Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
1	0.40	22.54	22.61	22.45	3.943	3.796	4.046
2	0.45	22.13	22.19	22.04	3.795	3.644	3.903
3	0.50	21.68	21.73	21.59	3.627	3.472	3.741
4	0.55	21.22	21.27	21.13	3.442	3.282	3.565
5	0.60	20.75	20.78	20.65	3.241	3.073	3.373
6	0.65	20.26	20.29	20.16	3.021	2.841	3.163
7	0.70	19.78	18.80	19.67	2.788	2.596	2.940
8	0.75	19.32	19.32	19.21	2.541	2.337	2.706
9	0.80	18.89	18.89	18.77	2.280	2.058	2.463
10	0.85	18.54	18.53	18.42	2.054	1.827	2.279
11	0.90	18.21	18.17	18.07	1.904	1.617	2.130
12	0.95	17.86	17.81	17.72	1.692	1.377	1.942
13	1.00	17.20	17.13	17.05	27.17	27.33	26.93

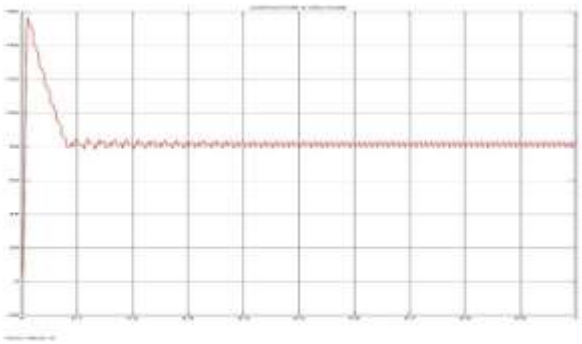

Fig.4.11: Output wave forms of capacitor voltages C1 balanced by ANN controller.

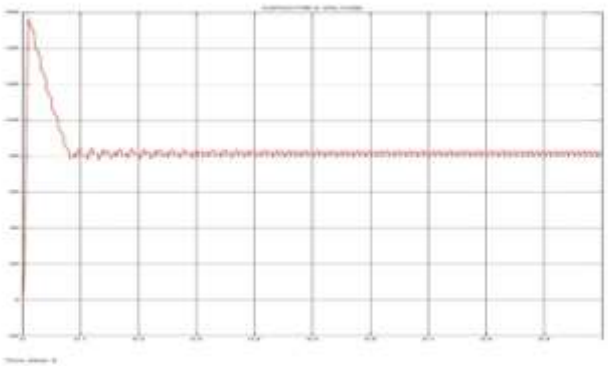

Fig.4.12: Output wave forms of capacitor voltages C2 balanced by ANN controller.

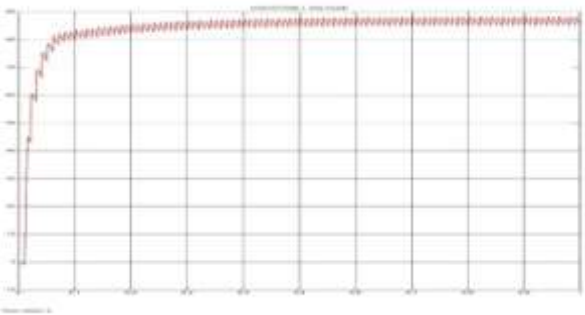

Fig.4.13: Output wave forms of capacitor voltages C3 balanced by ANN controller.

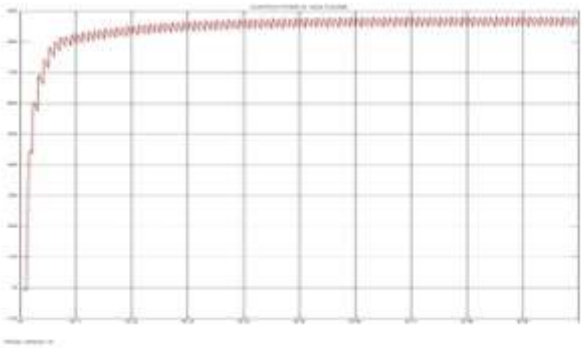

Fig.4.14: Output wave forms of capacitor voltages C4 balanced by ANN controller.

V. CONCLUSION

Proportional plus Integral based Control scheme and ANN based control scheme for capacitor voltage balancing are analyzed and modeled. The circuits thus modeled are applied to TLBC based five-level neutral point clamped inverter.The performance of

the control schemes are compared when the converter is supplying both balanced and unbalanced loads.It has been observed that ANN based gives a better transient as well as study state response when compared with PI controller and achieves.With the help of the proposed ANN controller, voltage balancing of capacitors can be done in better manner.

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